CPRE 4910 Weekly Report 01

8/25/2025 – 9/18/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Verification Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**
  - This week we scoped our project, grew the team, created the design document, wrote the problem statement, spoke to industry professionals

- **Past week accomplishments**
  - Colin McGann: Worked on a high-level design diagram to give a better idea of how the design should continue. Worked on taping out a design for Chipforge which contains components that will be useful for our future goals. Also got the bus ready for others to use.
  - Michael Drobot: Created requirements document and filled in project deliverables and requirements. Created design document and filled in initial hardware and software implementation details and architecture plans.
  - Samuel Forde: Studied pipelined graphics architectures and worked on chipforge tutorials.

- Jack Tonn: Created list of possible users for an ASIC GPU, wrote the problem statement, gained background knowledge on graphics hardware and software systems.
- Dawud Benedict: Researched GPU pipeline and architecture. Continued working with toolchain and getting a simple example adder build using the logic-analyzer pins. Looking into UVM or other verification methods with Jack.
- Emil Kosic: Worked through chip forge tutorials to familiarize with the tools we will use.
- Joshua Arceo: Worked through chip forge tutorials to familiarize with the tools we will use.

- **Pending issues**
  - N/A
- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Colin McGann	Chipforge tapeout, high-level diagram	20 :(	20
Michael Drobot	Design doc, requirements doc	4	4
Samuel Forde	Toolchain tutorials, documents, related reading	4	4
Jack Tonn	Problem Statement, Paperwork, User definitions	5	5
Dawud Benedict	Adder user-project, research	4	4
Emil Kosic	Familiarized self with relevant tools	3	3
Joshua Arceo	Familiarized self with relevant tools	3	3

- **Comments and extended discussion** *(Optional)*
  Feel free to discuss non-technical issues related to your project.

- **Plans for the upcoming week** *(Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.)*
  - Colin McGann: Refine my diagram and start working on the bus
  - Michael Drobot: Finalize the architecture plan, start making hardware PMODs.
  - Samuel Forde: Continue to do research on different pipelined methods and help with user definitions.
  - Jack Tonn: Look into verification methods, compare and contrast them to make a choice on what to use for this project. Continue to work on project statement and user definitions.

- Dawud Benedict: Finish my example so I can actually start on a useful implementation. Possibly start testbenches. Help Jack with verification method chosen.
- Emil Kosic: Look into other verification methods, continue to do chipforge tutorials. Create coding standards.
- Joshua Arceo: Complete more Chipforge tutorials, begin looking into which areas I can contribute the most into

- **Summary of weekly advisor meeting**
  - Met with advisor twice over report's period, and went through introductions, explained our general plans for how we would like to approach the project. Additionally, Dr. Duwe conveyed that he wanted this project to have a proper verification process, and that we scope the project this week.